What Is Claimed Is:

1. A method for using electrostatic forces to align semiconductor chips relative to each other, comprising:

electrically charging a first set of conductors on a first chip;

electrically charging a second set of conductors on a second chip;

placing the first chip face-to-face with the second chip, so that the first set of conductors is in close proximity to the second set of conductors; and

allowing electrostatic forces between the first set of conductors and the second set of conductors to bring the first chip into alignment with the second chip.

2. The method of claim 1, wherein the process of electrically charging the first set of conductors and the second set of conductors takes place after the first chip is placed face-to-face with the second chip.

3. The method of claim 1, wherein the process of electrically charging the first set of conductors and the second set of conductors involves applying a changing pattern of voltages to the first set of conductors and the second set of conductors.

4. The method of claim 1, further comprising vibrating the first chip and/or the second chip to facilitate aligning the first chip and the second chip.

5. The method of claim 1, further comprising applying a lubricant between the first chip and the second chip to reduce frictional forces between the first chip and the second chip during the alignment process.

6. The method of claim 1, wherein placing the first chip face-to-face with the second chip involves using a mold as a guide to facilitate bringing the first set of conductors in close proximity to the second set of conductors.

7. The method of claim 1, wherein a pattern formed by the first set of conductors matches a pattern formed by the second set of conductors.

8. The method of claim 1, wherein the first set of conductors and the second set of conductors are arranged in a checkerboard pattern.

9. The method of claim 1, wherein the first set of conductors and the second set of conductors are arranged in a pattern of concentric circles.

10. The method of claim 1, wherein the first set of conductors and the second set of conductors are arranged in a pattern with an autocorrelation approaching an impulse.

11. The method of claim 1, wherein the electrostatic forces between the first set of conductors and the second set of conductors include attractive forces and/or repulsive forces.

12. The method of claim 11, wherein the electrostatic forces between the first set of conductors and the second set of conductors generate a net repulsive force that levitates the first chip over the second chip, thereby reducing frictional forces between the first chip and the second chip.

13. The method of claim 1, wherein the first set of conductors comprises part of a power network and/or a ground network of the first chip.

14. The method of claim 1, wherein electrically charging the first set of conductors on the first chip involves charging different conductors to different voltage levels.

15. The method of claim 1, wherein electrically charging the first set of conductors involves using electron-implanted charges.

16. The method of claim 1, further comprising bonding the first chip with the second chip after the first chip is brought into alignment with the second chip.

17. An apparatus that facilitates using electrostatic forces to align semiconductor chips relative to each other, comprising:

a charging mechanism configured to electrically charge a first set of conductors on a first chip and a second set of conductors on a second chip; and

an initial placement mechanism configured to place the first chip face-to-face with the second chip, so that the first set of conductors is in close proximity to the second set of conductors;

whereby electrostatic forces between the first set of conductors and the second set of conductors bring the first chip into alignment with the second chip.

18. The apparatus of claim 17, wherein the charging mechanism operates after the first chip is placed face-to-face with the second chip.

19. The apparatus of claim 17, wherein the charging mechanism applies a changing pattern of voltages to the first set of conductors and the second set of conductors.

20. The apparatus of claim 17, further comprising a vibrating mechanism configured to vibrate the first chip and/or the second chip to facilitate aligning the first chip and the second chip.

21. The apparatus of claim 17, further comprising a lubricating mechanism configured to apply a lubricant between the first chip and the second chip to reduce frictional forces between the first chip and the second chip during the alignment process.

22. The apparatus of claim 17, wherein the initial placement mechanism is configured to use a mold as a guide to facilitate bringing the first set of conductors in close proximity to the second set of conductors.

23. The apparatus of claim 17, wherein a pattern formed by the first set of conductors matches a pattern formed by the second set of conductors.

24. The apparatus of claim 17, wherein the first set of conductors and the second set of conductors are arranged in a checkerboard pattern.

25. The apparatus of claim 17, wherein the first set of conductors and the second set of conductors are arranged in a pattern of concentric circles.

26. The apparatus of claim 17, wherein the first set of conductors and the second set of conductors are arranged in a pattern with an autocorrelation approaching an impulse.

27. The apparatus of claim 17, wherein the electrostatic forces between the first set of conductors and the second set of conductors include attractive forces and/or repulsive forces.

28. The apparatus of claim 27, wherein the electrostatic forces between the first set of conductors and the second set of conductors generate a net repulsive force that levitates the first chip over the second chip, thereby reducing frictional forces between the first chip and the second chip.

29. The apparatus of claim 17, wherein the first set of conductors comprises part of a power network and/or a ground network of the first chip.

30. The apparatus of claim 17, wherein the charging mechanism is configured to charge different conductors to different voltage levels.

31. The apparatus of claim 17, wherein the charging mechanism is configured to use electron-implanted charges.

32. The apparatus of claim 17, further comprising a bonding mechanism that is configured to bond the first chip with the second chip after the first chip is brought into alignment with the second chip.

33. A means for using electrostatic forces to align semiconductor chips relative to each other, comprising:

a charging means for electrically charging a first set of conductors on a first chip and a second set of conductors on a second chip; and

an initial placement means for placing the first chip face-to-face with the second chip, so that the first set of conductors is in close proximity to the second set of conductors;

whereby electrostatic forces between the first set of conductors and the second set of conductors bring the first chip into alignment with the second chip.